

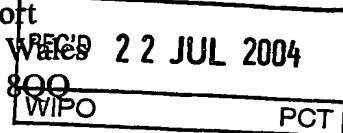
BEST AVAILABLE COPY



INVESTOR IN PEOPLE

GB04/2600

The Patent Office
Concept House
Cardiff Road
Newport
South Wales NP10 8QQ



**PRIORITY
DOCUMENT**
SUBMITTED OR TRANSMITTED IN
COMPLIANCE WITH RULE 17.1(a) OR (b)

I, the undersigned, being an officer duly authorised in accordance with Section 74(1) and (4) of the Deregulation & Contracting Out Act 1994, to sign and issue certificates on behalf of the Comptroller-General, hereby certify that annexed hereto is a true copy of the documents as originally filed in connection with the patent application identified therein.

In accordance with the Patents (Companies Re-registration) Rules 1982, if a company named in this certificate and any accompanying documents has re-registered under the Companies Act 1980 with the same name as that with which it was registered immediately before re-registration save for the substitution as, or inclusion as, the last part of the name of the words "public limited company" or their equivalents in Welsh, references to the name of the company in this certificate and any accompanying documents shall be treated as references to the name with which it is so re-registered.

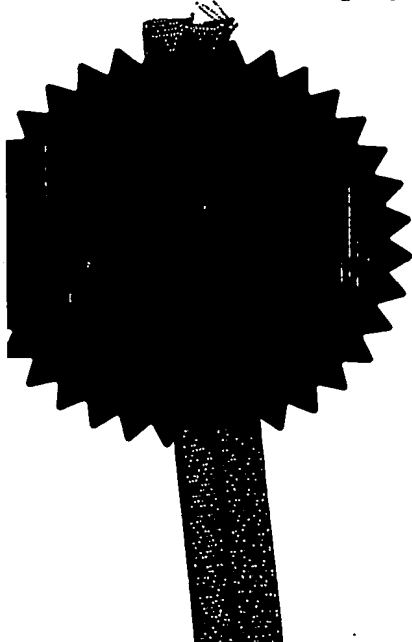
In accordance with the rules, the words "public limited company" may be replaced by p.l.c., plc, P.L.C. or PLC.

Re-registration under the Companies Act does not constitute a new legal entity but merely subjects the company to certain additional company law rules.

Signed

Stephen Hordley

Dated 8 July 2004



27 JUN 2003

27JUN03 0818319-1 002005
P01/7700 0.00 0314999.4

NEWPORT

Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

The Patent Office

Cardiff Road
Newport
South Wales
NP9 1RH

1. Your reference	XA1731		
2. Patent application number (The Patent Office will fill in this part)	0314999.4		27 JUN 2003
3. Full name, address and postcode of the or of each applicant (underline all surnames)	BAE SYSTEMS plc 6 Carlton Gardens London, SW1Y 5AD United Kingdom Patents ADP number (if you know it) If the applicant is a corporate body, give the country/state of its incorporation United Kingdom		
4. Title of the invention	IMPROVEMENTS IN OR RELATING TO THE OPERATIONAL FREQUENCY RANGE OF LATCH CIRCUITS		
5. Name of your agent (if you have one)	"Address for service" in the United Kingdom to which all correspondence should be sent (including the postcode) Patents ADP number (if you know it)		
	BAE SYSTEMS plc Group IP Department Lancaster House, P.O. Box 87 Farnborough Aerospace Centre Farnborough, Hampshire, GU14 6YU 07914674002 ✓		
6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and (if you know it) the or each application number	Country	Priority application number (if you know it)	Date of filing (day / month / year)
7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application	Number of earlier application		Date of filing (day / month / year)
8. Is a statement of inventorship and of right to grant of a patent required in support of this request? (Answer 'Yes' if: a) any applicant named in part 3 is not an inventor, or b) there is an inventor who is not named as an applicant, or c) any named applicant is a corporate body. See note (d))	YES		

Patents Form 1/77

Enter the number of sheets for any of the following items you are filing with this form.
Do not count copies of the same document

Continuation sheets of this form

Description	05
Claim(s)	01
Abstract	01
Drawing(s)	05

10. If you are also filing any of the following, state how many against each item.

Priority documents

Translations of priority documents

Statement of inventorship and right to grant of a patent (*Patents Form 7/77*)

Request for preliminary examination and search (*Patents Form 9/77*)

1

Request for substantive examination (*Patents Form 10/77*)

Any other documents
(please specify)

11.

I/We request the grant of a patent on the basis of this application.

Signature

Margaret Mackett

Date

25 June 2003

12. Name and daytime telephone number of person to contact in the United Kingdom

Maria Burkes 01252 383487

Warning

After an application for a patent has been filed, the Comptroller of the Patent Office will consider whether publication or communication of the invention should be prohibited or restricted under Section 22 of the Patents Act 1977. You will be informed if it is necessary to prohibit or restrict your invention in this way. Furthermore, if you live in the United Kingdom, Section 23 of the Patents Act 1977 stops you from applying for a patent abroad without first getting written permission from the Patent Office unless an application has been filed at least 6 weeks beforehand in the United Kingdom for a patent for the same invention and either no direction prohibiting publication or communication has been given, or any such direction has been revoked.

Notes

- If you need help to fill in this form or you have any questions, please contact the Patent Office on 0645 500505.
- Write your answers in capital letters using black ink or you may type them.
- If there is not enough space for all the relevant details on any part of this form, please continue on a separate sheet of paper and write "see continuation sheet" in the relevant part(s). Any continuation sheet should be attached to this form.
- If you have answered 'Yes' Patents Form 7/77 will need to be filed.
- Once you have filled in the form you must remember to sign and date it.
- For details of the fee and ways to pay please contact the Patent Office.

DUPLICATE

- 1 -

IMPROVEMENTS IN OR RELATING TO THE OPERATIONAL FREQUENCY RANGE OF LATCH CIRCUITS

The present invention relates to improvements in or relating to the operational frequency range of latch circuits and is more particularly, although
5 not exclusively, concerned with improvements relating to 'hold/follow' latches.

It is common to use a 'divide-by-2' prescaler in many types of circuits. These prescalers consist of two latches, namely, a master latch and a slave latch, both latches changing their modes to either holding or following in accordance with input clock phase. Such latches are generally known as
10 'hold/follow' latches.

However, prescalers tend to have a maximum toggle rate or frequency due to their construction. In particular, the maximum toggle rate or frequency tends to be governed by the transistors used to implement the 'hold/follow' latches, the layout parasitics and track path lengths.

15 It is therefore an object of the present invention to provide an improved prescaler, which has a higher maximum toggle rate.

In accordance with one aspect of the present invention, there is provided a latch circuit including:-

a first latch portion including a first clock transistor; and
20 a second latch portion including a second clock transistor;

wherein the first and second clock transistors form a transistor clock pair and the first clock transistor has a different property or characteristic to the second clock transistor such that the 'hold period/follow period' ratio of the transistor clock pair is greater than 1.

25 Advantageously, the different property or characteristic comprises a difference in emitter area.

Preferably, the emitter area of the first clock transistor is greater than that of the second clock transistor.

In one embodiment, the emitter area of the first clock transistor is double that of the second clock transistor.

In accordance with another aspect of the present invention, there is provided a prescaler circuit including a first and second latch circuit as
5 described above.

For a better understanding of the present invention, reference will now be made, by way of example only, to the accompanying drawings in which:-

Figure 1 illustrates a known 'divide-by-2' prescaler;

Figure 2 illustrates the clock signals applied to the Figure 1 prescaler and
10 the outputs of the master and slave latches thereof;

Figure 3 illustrates a latch circuit in more detail;

Figure 4 illustrates a latch circuit in accordance with the present invention; and

Figure 5 illustrates the relative sensitivities of the Figure 3 and Figure 4
15 latches.

Referring initially to Figure 1, a typical 'divide-by-2' prescaler 10 is shown which comprises a master latch 12 and a slave latch 14. Each latch 12, 14 is connected to receive clock inputs 16, 18 along lines 20, 22 and 24, 26 respectively. Clock inputs 16 and 18 are complementary, and when clock input
20 16 is high, clock input 18 is low and vice versa. The latches 12, 14 are connected together by lines 28, 30 as shown, and are also connected to outputs 32, 34 via respective lines 36, 38 and 40, 42. Lines 40 and 42 comprise the outputs from latch 14 and lines 28 and 30 comprise the outputs from latch 12.

When the clock input 16 to a latch 12 is high and the clock input 18 is
25 low, the data output of latch 12 follows on lines 28 and 30 and the data output of latch 14 holds its current state, that is, the current data. When the clock input 16 is low and the clock input 18 is high, latch 12 holds its current state and latch 14 follows the data. For the prescaler 10 shown in Figure 1, the outputs 32, 34 toggle their states on the falling edge of clock input 16 as shown in Figure 2.

In Figure 2, the waveforms of the clock inputs 16, 18 are shown. The waveforms for the outputs 32, 34 are also shown. Line 44 indicates that the outputs 34 toggles on the falling edge of clock input 16.

Figure 3 illustrates a latch circuit 50. The latch circuit 50 can be used for both the master and the slave latches 12, 14 of Figure 1. The circuit 50 includes complementary clock inputs 52, 54 and outputs 56, 58, and is divided into a left portion 60 and a right portion 62. A plurality of bipolar transistors 64, 66, 68, 70, 72, 74, 76, 78, 80, 82 are provided together with three capacitors 84, 86, 88, two resistors 90, 92 and five current sources 94, 96, 98, 100, 102. The transistors 64, 66, 68, 70, 72, 74, 76, 78, 80, 82, resistors 90, 92 and current sources 94, 96, 98, 100, 102 are connected in a known way to carry out the latching function. The capacitors 84, 86, 88 are shown to represent layout 'parasitics' which are typical in a high frequency integrated circuit (IC). These should be minimised to increase toggle rate. The term 'layout 'parasitic"' is well known in this field.

The transistors have been described as being bipolar transistors. They may be both heterojunction or homojunction bipolar transistors.

In Figure 3, each resistor 90, 92 has the same resistance value. Similarly, all the transistors 64, 66, 68, 70, 72, 74, 76, 78, 80, 82 have the same emitter area of $4\mu\text{m}^2$. It is to be noted that it is not essential that the values be those illustrated.

In the arrangement shown in Figure 3, transistors 76, 78 receiving the complementary clock inputs 52, 54 are generally known as a transistor clock pair. The transistor clock pair as shown here is said to be 'balanced', that is, the 'hold/follow' ratio for the latch circuit 50 is 1. The maximum toggle rate or frequency of circuit 50 where it can still just about perform the 'divide-by-2' function is around 12.2GHz.

It has been found that by doubling the emitter area of transistor 76 to $8\mu\text{m}^2$ and leaving all the other values the same, an improved maximum toggle rate and frequency gain flatness can be obtained as the 'hold/follow' ratio increases.

Figure 4 illustrates an improved latch circuit 110 which provides the improved maximum toggle rate. Components which are identical to those already described with reference to Figure 3 are referenced alike. The circuit 110 includes complementary clock inputs 52, 54 as before and has outputs 112, 114, and is divided into a left portion 116 and a right portion 62. Left portion 116 of Figure 4 differs from left portion 60 of Figure 3 as it includes a transistor 118 which has a larger emitter area than transistor 76. As before, transistors 118, 78 form a transistor clock pair and receive clock inputs 52, 54. As transistor 118 has a larger emitter area than transistor 76, the transistor clock pair is said to be 'imbalanced' as the 'hold period/follow period' ratio is now greater than 1. This has the effect of increasing the maximum toggle rate to 14GHz as shown in Figure 5.

In Figure 5, a comparison of the respective sensitivity of latch circuits 50, 110 against input frequency is shown. The sensitivity of the latch circuit 50 is indicated by line 120 and the sensitivity of the latch circuit 110 is indicated by line 122. The self-resonance for the left portion 60, 116 for each latch circuit 50, 110 is indicated by portions 124, 126 respectively of the lines 120, 122. In these regions, the respective left portion 60, 116 is at its most sensitive. It can readily be seen that the self-resonance increases from around 9GHz to 12GHz.

For applications which require operation below self-resonance, the latch circuit 110 of Figure 5 provides substantial benefits. For an operational sensitivity of between -20dBm and -30dBm, line 120 shows that the conventional latch circuit 50 has an operational region extending between markers 124, 126 of around between 2GHz and 7GHz giving a 5GHz bandwidth. For the same operational sensitivity, line 122 shows that the improved latch circuit 110 has an operational region extending between markers 128, 130 of around between 2GHz and 10.5GHz giving a 8.5GHz bandwidth. This represents an improvement in operational bandwidth of around 70%.

As mentioned above, the master and slave latches 12, 14 are currently implemented by latch circuit 50 of Figure 3. By replacing latch circuit 50 with latch circuit 110 in prescaler 10, significant improvements can be made to the

maximum toggle rate or frequency of the prescaler 10 without incurring an increase in current consumption or the number of transistors. Additionally, the self-resonance of the prescaler can also be increased.

5 It will readily be appreciated that, although the invention has been described such that the emitter area of transistor 118 is twice that of transistor 78, it is not limited to this value. The emitter area of transistor 118 can be any suitable multiple of the emitter area of transistor 78 greater than 1 to provide an increased maximum toggle rate or frequency and 'hold/follow' ratio. Naturally, the emitter area of transistor 118 will be chosen in accordance with the
10 particular application.

Although the present invention has been described with reference to bipolar transistors having a change in emitter area to provide the increased maximum toggle rate or frequency and 'hold/follow' ratio, it will be understood that the same principle can also be applied to field effect transistors (FETs). In
15 this case, one or more properties or characteristics of the FET may be changed to provide the increased maximum toggle rate or frequency and 'hold period/follow period' ratio.

It will be appreciated that the benefits discussed above can easily be mapped to a higher yield of integrated circuits for a required performance with
20 an accompanying reduction in production costs.

CLAIMS:

1. A latch circuit including:-
a first latch portion including a first clock transistor; and
a second latch portion including a second clock transistor;
- 5 wherein the first and second clock transistors form a transistor clock pair and the first clock transistor has a different property or characteristic to the second clock transistor such that the 'hold period/follow period' ratio of the transistor clock pair is greater than 1.
2. A latch circuit according to claim 1, wherein the different property or
10 characteristic comprises a difference in emitter area.
3. A latch circuit according to claim 2, wherein the emitter area of the first clock transistor is greater than that of the second clock transistor.
4. A latch circuit according to claim 3, wherein the emitter area of the first clock transistor is double that of the second clock transistor.
- 15 5. A prescaler circuit including a first and second latch circuit according to any one of the preceding claims.
6. A latch circuit substantially as hereinbefore described with reference to Figures 4 and 5 of the accompanying drawings.
7. A prescaler circuit substantially as hereinbefore described.

ABSTRACT

IMPROVEMENTS IN OR RELATING TO CIRCUIT PERFORMANCE

Described herein is a latch circuit (110) which has an improved maximum toggle rate or frequency. The latch circuit (110) comprises a first portion (116) and a second portion (62) in which input clock signals (52, 54) are applied to respective input transistors (118, 78). The input transistor (118) for the first portion (116) has an emitter area which is double that of the input transistor (78) for the second portion (62). This 'imbalance' between the two input transistors (118, 78) provides an increase in the 'hold period/follow period' ratio such that it is greater than 1, the self-resonance of the latch circuit (110) and also maximum toggle rate or frequency.

(Fig. 4)

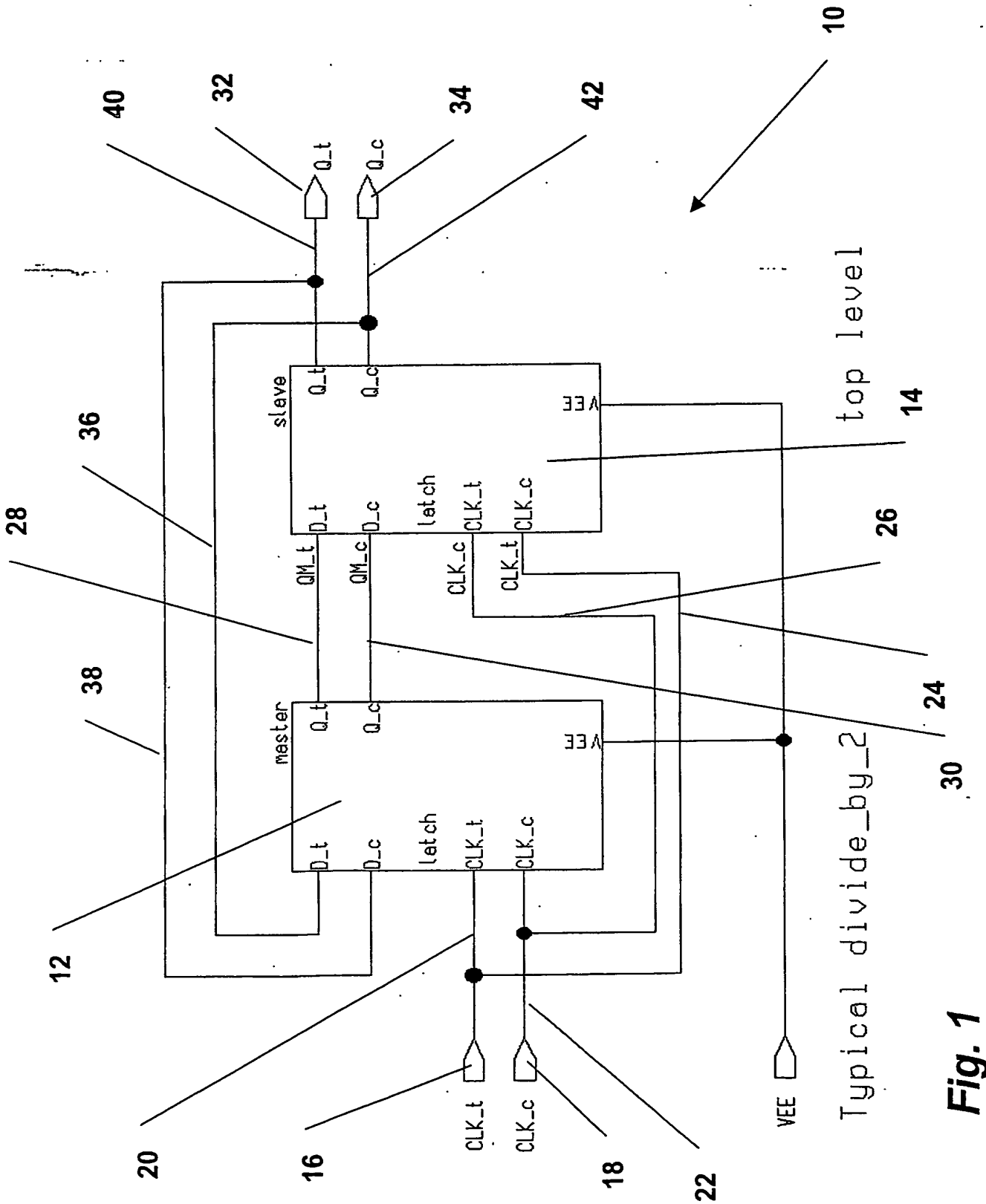


Fig. 1

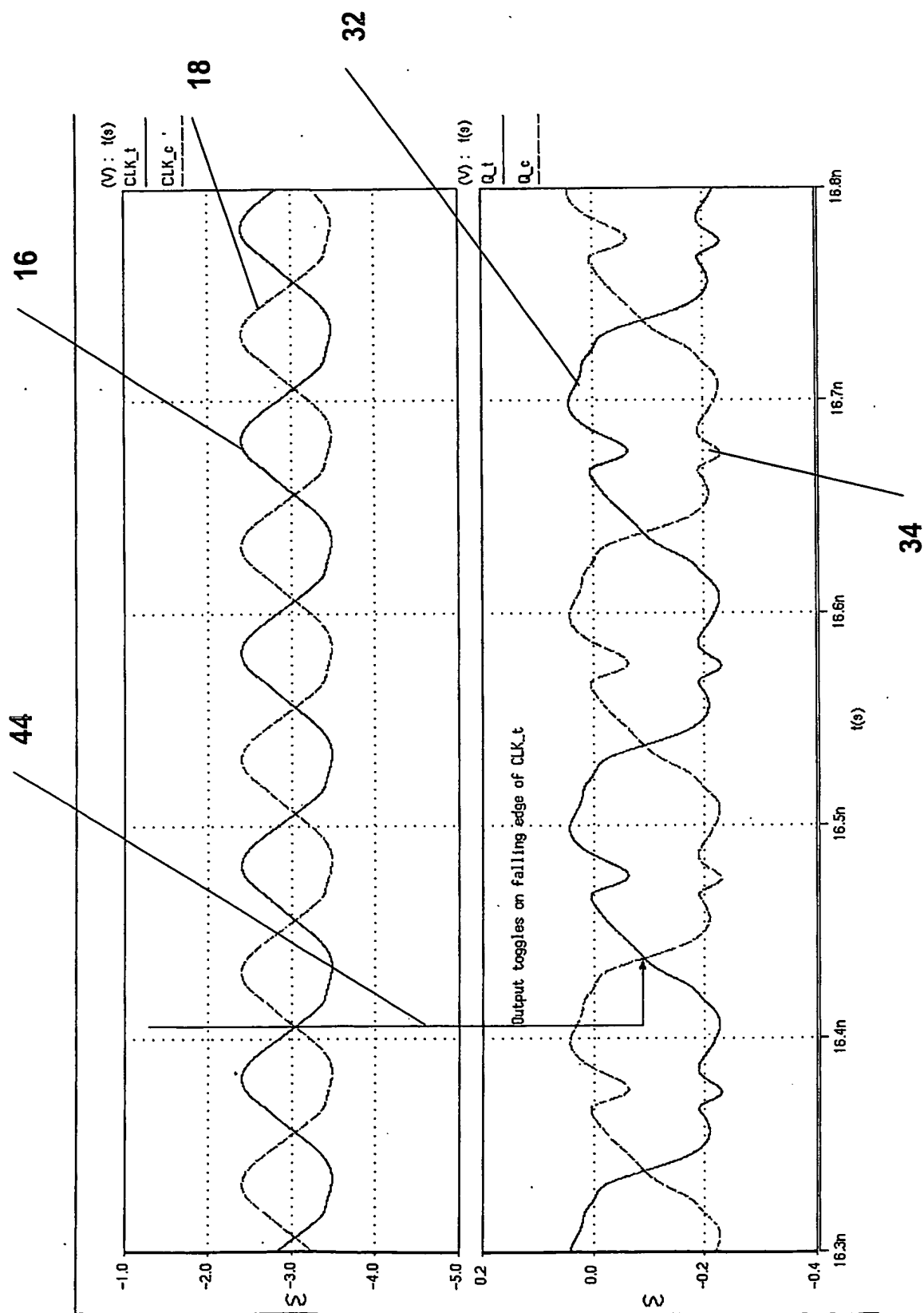


Fig. 2

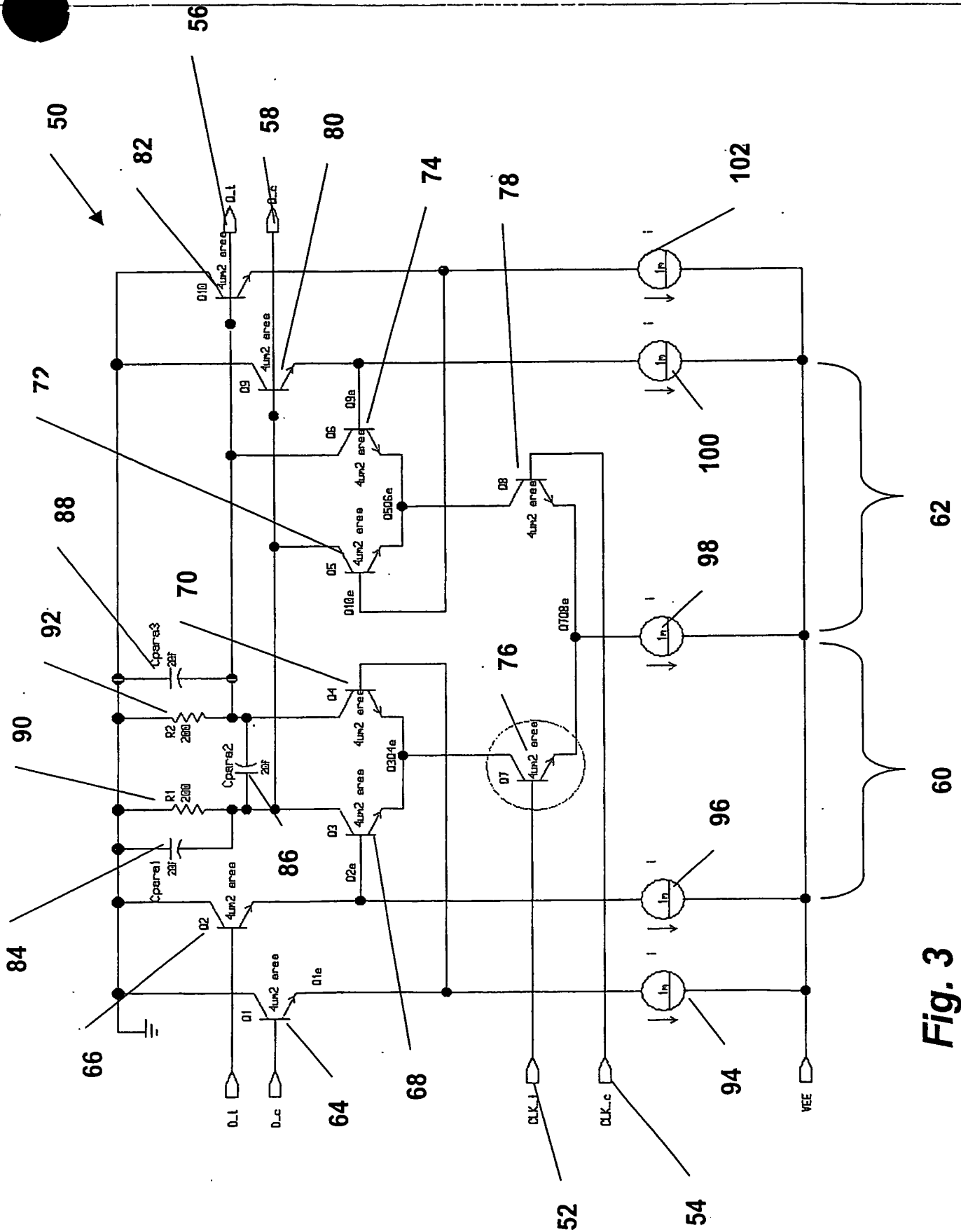


Fig. 3

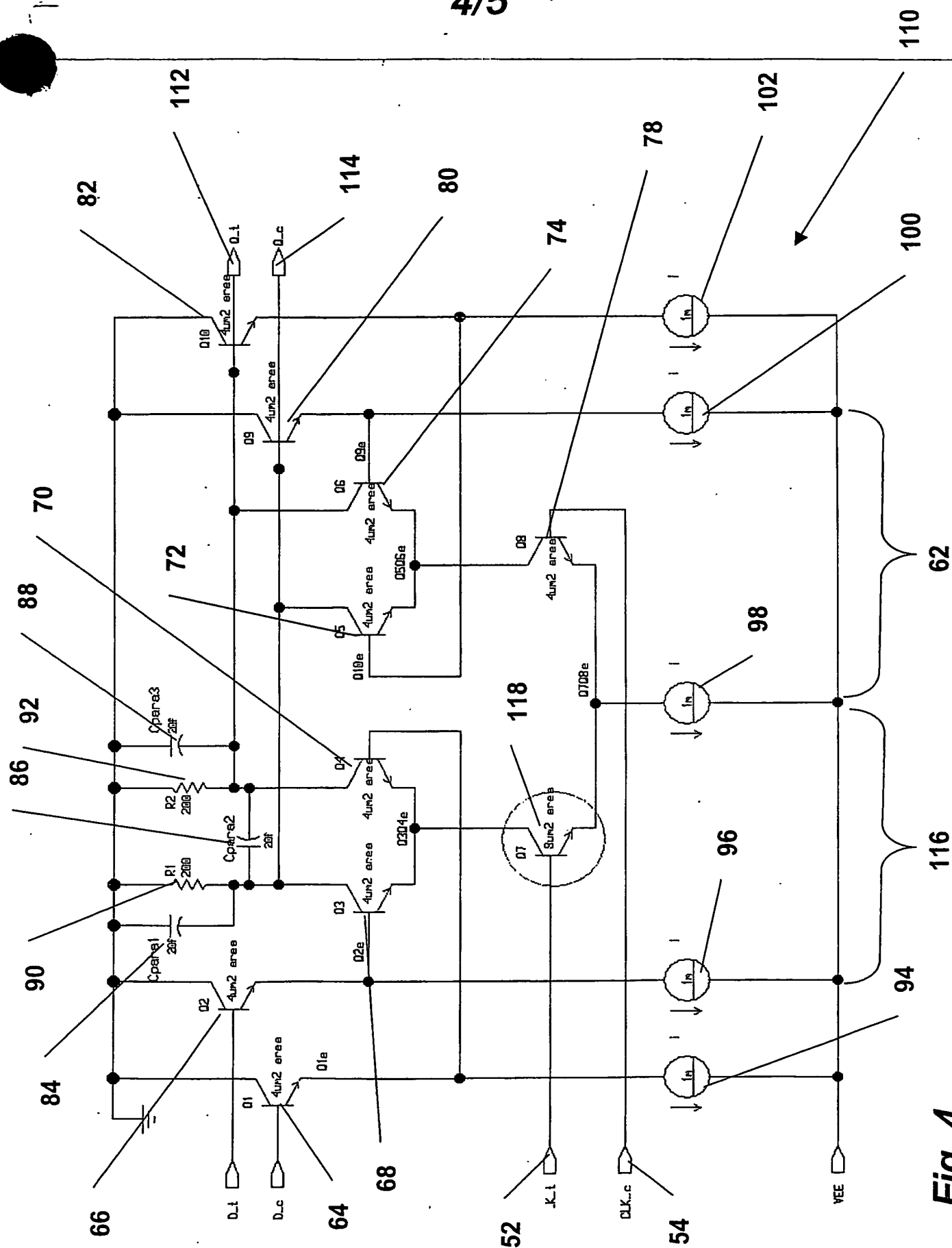


Fig. 4

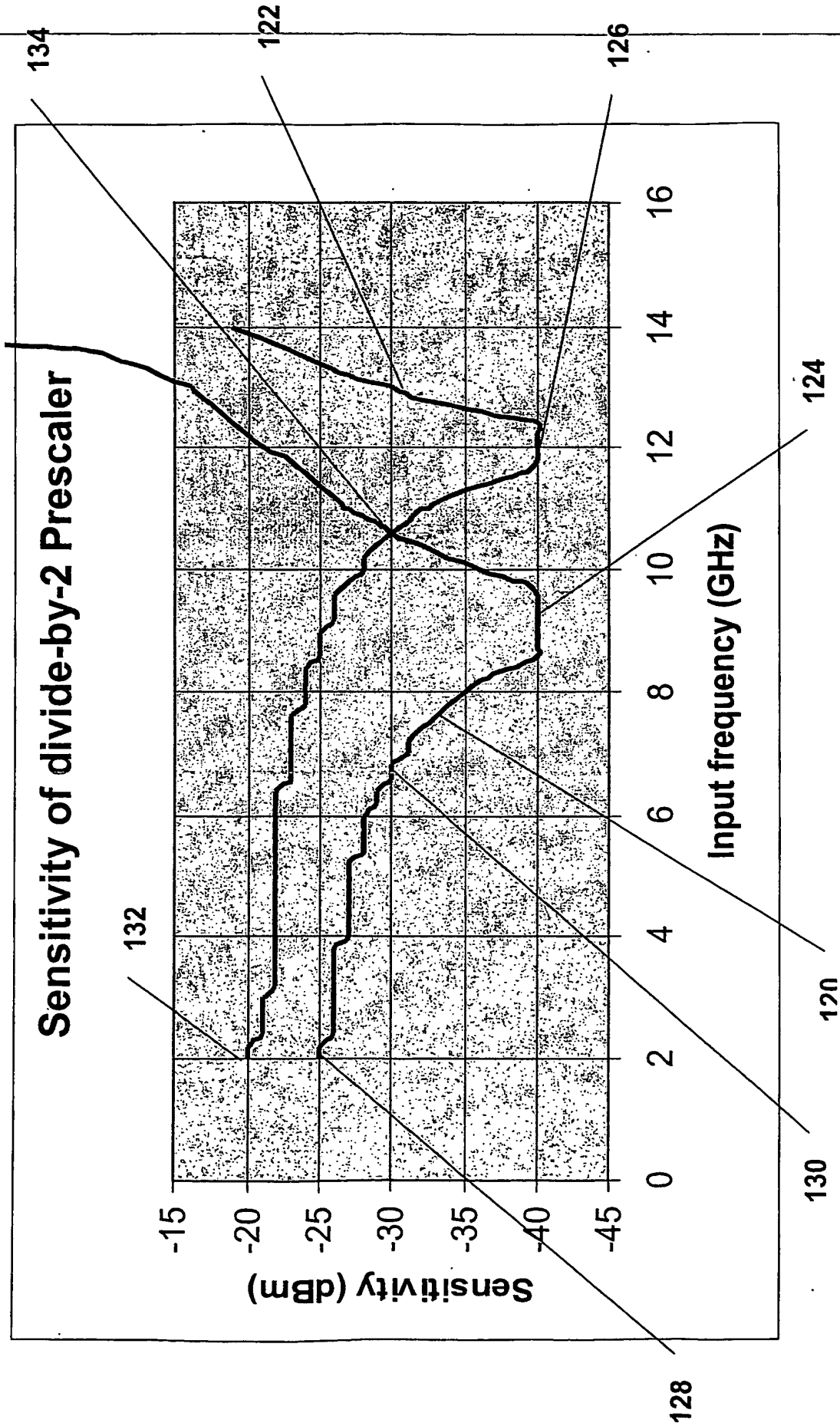


Fig. 5

PCT/GB2004/002600



THE PATENT OFFICE

08 JUL 2004

**Received in Patents
International Unit**

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☒ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.